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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,183	07/21/2004	Hendricus Joseph Maria Veendrick	NL020066	5511

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CAVALLARI, DANIEL J	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,183	VEENDRICK ET AL.	
	Examiner	Art Unit	
	Daniel J. Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/21/04 & 4/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 7/21/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The information disclosure statement (IDS) submitted on 4/18/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Component 230 of Figure 2 is not explained in the specification.

Appropriate action is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a single enabling transistor, does not reasonably provide enablement for two enabling transistor. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

Claim 1 enables for a single enabling transistor "an enabling transistor for coupling the internal power supply line to the external power supply line." However, the limitation "...by biasing the second gate voltage" is not enabled as it suggests a second gate of the enable transistor. The limitation of is not clear as it suggests a second gate and a voltage itself cannot be biased but rather a transistor is biased by a biasing voltage. The claim will be examined as best understood in which only one enable transistor is used, as disclosed in Figure 1, and two gate control voltages are present in which a second control voltage is used to bias the gate of the enable transistor.

Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 2 recites the limitation of "a transistor (154) having a substrate that is conductively insulated from a bulk substrate of the integrated circuit, the substrate being coupled to a bias voltage source (170)..." However, Figure 1 shows only the gate of transistor (154) connected to the bias voltage source (170) for response to the control signal (160) and connection to the supply line (140) and the external power supply Vss (130). Figure 1 fails to show a connection between the source (170) and the substrate of transistor (154) and it's insulation from the bulk substrate.

The claim will be examined as best understood in which a source is used to create a greater voltage at power supply (130) and a lower voltage at power supply (140) and respond to a control signal (160).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ye et al. (US 6,329,874 B1)

Ye et al. teaches:

In regard to Claim 1

- An external power supply line (GND)
- An internal power supply line (VGD)
- A circuit (240) coupled to the internal power supply (VGD) and a transistor (L1) for coupling the circuit to the external power supply line (GND)
- Control means (305, T1, T2, & 315) coupled to the gate of the enable transistor (L1) for switching the transistor to a conductive state with a first gate voltage and a non-conductive state with a second gate voltage (See Column 5, Lines 9-37)

(See Figure 3)

In regard to Claims 2 &3

- The control means (305, T1, T2, & 315) comprising of a transistor (T2) connected to a bias voltage source read on by the charge pump (315) (See Column 4, Lines 37-53) and a transistor (T2) being responsive to a control signal (STDBY) for switching the enable transistor (L1) to a non-conductive state (See Column 5, Lines 8-21)

(See Figure 3)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al., Hoffman et al. (4,722,372).

Incorporating all arguments above of the power supply system taught by Ye et al. in which Ye et al. teaches a battery (232) powered device, read on by the computer system (200), and an external power supply line, read on by the bus (205) (See Figure 2). Ye et al. fails to explicitly teach a power supply line coupled to a contact of a battery container and also fails to explicitly teach the supply line coupled to an external power supply line of an integrated circuit.

Hoffman teaches an integrated circuit attached to the contacts (124f) of a battery container (126a) (See figure 20 & Column 11, Lines 47-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ye et al. incorporating the battery receptacle as taught by Hoffman incorporating contacts in which to connect the power supply line with the battery and provide power to the integrated circuit. The motivation would have been to create a container that would allow for easy access to that batteries in order to change or service the batteries as well as create a good electrical connection between the circuitry and the battery and provide a portable means of power to the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

October 12, 2005

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800